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UM10062

ISP1505 ULPI transceiver evaluation board, supporting Hi-Speed USB host and peripheral

Rev. 01 — 2 May 2006 User manual

Document information

Info	Content
Keywords	isp1505, usb, ulpi, universal serial bus, transceiver, utmi+ low-pin interface, host, peripheral, otg, usb 2.0, phy
Abstract	The document describes how the ISP1505 eval board can be configured to interface with link to provide a USB physical layer front-end solution. This document also includes the schematic of the eval board and the components needed to integrate the ISP1505 to the user's system.

PHILIPS

Revision history

Rev	Date	Description
01	20060502	First release.

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1. Introduction

The ISP1505 is an 8-bit bidirectional UTMI+ Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to implement as a Hi-Speed USB host or peripheral device.

The ISP1505 evaluation (eval) board allows designers to evaluate the features of the ISP1505, and conduct system-level validation and testing. The eval board interfaces to the link through a 100-pin Transceiver and Macrocell Tester (T&MT) connector that complies with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2*.

Fig 1 shows the ISP1505 eval board.

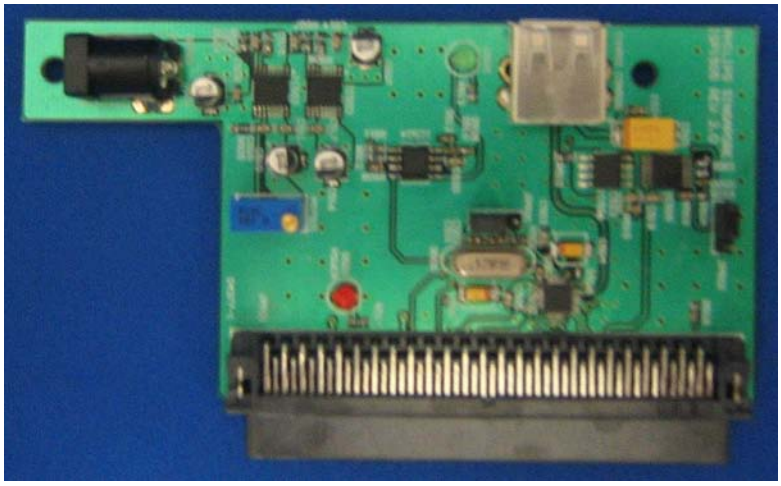

Fig 1. ISP1505 eval board

2. Board features

2.1 Functionality

- The ISP1505 is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1.*
- The T&MT connector interface is fully compliant with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2.*
- The on-board power switch can supply the V_{BUS} current.
- Configurable active-HIGH or active-LOW reset signal from the link.
- Adjustable V_{CC} voltage when powered by the 5 V DC power supply.
- Flexible clock source for the ISP1505: on-board crystal, 60 MHz input clock or square wave clock driven to the XTAL1 input.

2.2 Connectors

- USB connector: standard-A USB connector or standard-B connector
- T&MT connector to interface to the link
- Input power connector

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2.3 Power supplies

- Supplied by the 5 V DC power supply through the input power connector, or
- Supplied by the link through the T&MT connector

3. Board usage

3.1 Overview

The ISP1505 eval board is designed to connect to a link board through the T&MT connector for system validation as shown in Fig 2.

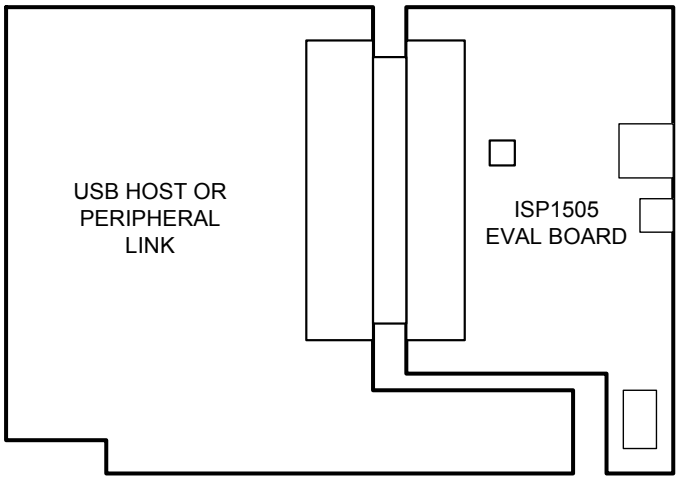

Fig 2. ISP1505 eval board connected to the link board

3.2 Block diagram

Fig 3 shows the high-level functional block diagram of the ISP1505 eval board.

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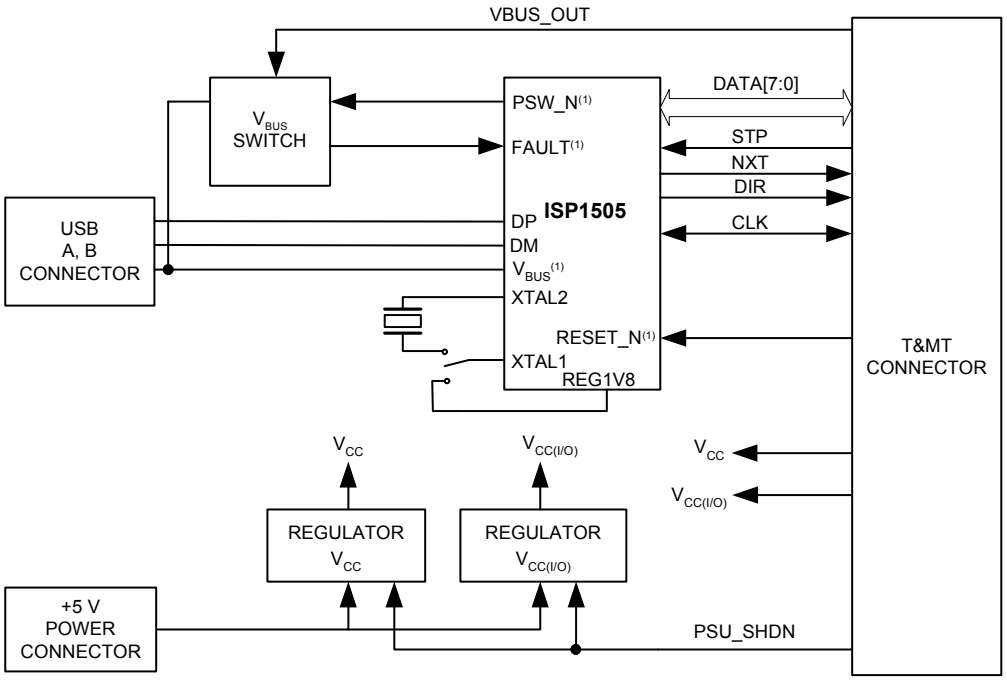

[1] These pins are multiplexed with other functions. Only one function, however, can be used at one time.

Fig 3. ISP1505 eval board functional block diagram

3.3 Power supply

The ISP1505 eval board can be powered either from the input power connector (SW500) or from the T&MT connector (JP501). When power is supplied from the link through the T&MT connector, pin 100 of the connector must be connected to ground on the link side. This will shut down the V_{CC} and $V_{CC(I/O)}$ regulator outputs to the ISP1505. When power is supplied from the input power connector, pin 100 of the T&MT connector must be left open on the link side.

There are two regulators on the eval board supplying V_{CC} and $V_{CC(I/O)}$. Regulator IC502 supplying V_{CC} has an adjustable output voltage, which must be set to a voltage between 3.0 V and 3.6 V by tuning POT501. Regulator IC503 supplying $V_{CC(I/O)}$ has a fixed output voltage of 3.3 V. Solder bridges S511 and S506 must always be closed. LED D501 indicates the existence of V_{CC}.

3.4 Clock supply

There are three ways to provide clock to the ISP1505:

- Attach a crystal between XTAL1 (pin 10) and XTAL2 (pin 11). In this case, a jumper must be placed between pin 1 and pin 2 of JP500. The value of the crystal depends on the silicon version.
- Drive a square wave clock signal into the XTAL1 pin. In this case, the jumper on pin 1 and pin 2 of JP500 must be removed and an external clock source is applied on pin 2 of JP500. The frequency of the external clock depends on the silicon version.
- Drive a 60 MHz clock signal into CLOCK (pin 21). In this case, the jumper on pin 1 and pin 2 of JP500 must be removed and 1.8 V must be applied to pin 2 of JP500 (the REG1V8 output can be connected to this pin). With 1.8 V applied to XTAL1, the

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CLOCK pin of the ISP1505 functions as an input on power-up and the link can drive 60 MHz clock into this pin.

3.5 Host application

A host is required to supply current to V_{BUS} and the current capability depends on the targeted application. An external charge pump or power switch is required to provide this current. According to *Universal Serial Bus Specification Rev. 2.0*, V_{BUS} can be continuously shorted to ground, without causing any damage. Therefore, the external charge pump or power switch must be able to detect overcurrent condition and thermally shut down the output. The ISP1505 can control the charge pump or power switch through the active-LOW open-drain output PSW_N (pin 12). V_{BUS} power switch MIC2026 (IC504) is implemented on the eval board as an example. To evaluate the ISP1505 for a host application, the eval board must be configured as follows:

1. Ensure that a standard-A USB connector is mounted on the eval board.
2. The link must provide 5 V DC to pin 28 of the T&MT connector.
3. Solder bridge S509 must be left open and solder bridge S508 must be closed. Therefore, pin 8 of the ISP1505 functions as a FAULT input, which is connected to the FLGA output of the power switch.
4. Solder bridges S500 and S501 must be left open and S507 must be closed. Therefore, pin 12 of the ISP1505 functions as a PSW_N output, controlling the power switch.
5. Solder bridges S510 and S502 must be closed and S512 must be left open. Therefore, the V_{BUS} pin of the standard-A connector is connected to the output of the power switch.

3.6 Peripheral application

High-speed devices do not provide current to V_{BUS}, instead sense the voltage on V_{BUS}. When the voltage on V_{BUS} rises above the session valid threshold, the device starts the function. Therefore, for a peripheral application, pin 8 of the ISP1505 functions as V_{BUS} and pin 12 functions as RESET_N. The eval board must be configured as follows:

1. Ensure that a standard-B USB connector is mounted on the eval board.
2. Open solder bridge S502 to reduce the V_{BUS} capacitance below 10 µF. Optionally, a 4.7 µF capacitor can be soldered between V_{BUS} and ground.
3. Open solder bridges S508 and S510 and close S509 to route V_{BUS} to pin 8 of the ISP1505.
4. Open solder bridge S507 to utilize pin 12 of the ISP1505 as a reset function. Open S500 and close S501 if the link provides an active-HIGH reset signal. Otherwise, open S501 and close S500.

3.7 Configuration summary

Table 1: summarizes the configuration of the eval board for host and peripheral applications.

Table 1: Configuration summary for host and peripheral applications

Configurable settings		Host application	Peripheral application
USB connector		standard-A	standard-B
V_{BUS} capacitance	S502	closed	open
	S509	open	closed

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Configurable settings		Host application	Peripheral application
	S510	closed	open
V_{BUS} power switch	S508	closed	open
	S507	closed	open
Reset control	S500	open	open
	S501	open	closed
V_{CC} power	S506	closed	closed
$V_{CC(I/O)}$ power	S511	closed	closed
Crystal selection	JP500	installed on pin 1 and pin 2	installed on pin 1 and pin 2

3.8 ESD protection

The ISP1505 has an internal ElectroStatic Discharge (ESD) protection diode that can withstand ±2 kV on the DP, DM and V_{BUS} pins. Therefore, an external protection diode is not required if ±2 kV ESD protection is enough for the application.

IC501 is an external protection diode, which is not mounted on the board.

3.9 Pull-up resistor on DM

This section describes how to configure the eval board as a low-speed peripheral. For low-speed peripheral application, DM is pulled up in the idle state. This can be achieved by enabling the external 1.5 kΩ pull-up resistor, using controller LS_Enable (pin 20 of JP501). Inverter IC505A is required if the low-speed enable is active HIGH because the gate of the PMOS switch must be LOW to route 3.3 V to the pull-up resistor. Solder bridges S504 and S505 provide the flexibility to bypass or use the inverter. Header JP502 allows to manually control the DM switching, without the low-speed enable.

4. Quick troubleshooting guide

Following is a step-by-step guide to troubleshoot the ISP1505 eval board, if you encounter any problem.

1. Check the printing on the IC package to ensure that you have the latest revision. The last letter on the third line indicates the revision of the chip.
2. Power the eval board through the SW500 connector with a 5 V power supply.
3. Measure the voltage at V_{CC}. It must be between 3.0 V and 3.6 V. Measure the voltage at $V_{CC(I/O)}$. It must be around 3.3 V. If both regulators give no output, check whether PSU_SHDN is pulled up to 5 V. If only one regulator gives abnormal output, it is likely that the regulator is faulty.
4. Measure the voltage at the RREF pin of the ISP1505. The voltage must be around 1.2 V. If the voltage at the pin is abnormal, it is likely that the chip is not properly soldered on the PCB or the IC is damaged. The 12 kΩ resistor connected to RREF provides the biasing for the whole chip. The voltage at the RREF pin must be checked first before further testing.
5. Measure the output voltage at REG1V8 and REG3V3. These voltages must be 1.8 V and 3.3 V, respectively. If the voltage at these pins is abnormal, it is likely that the IC is damaged.
6. Check jumper and solder bridge settings according to the target application given in Table 1:.

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7. Probe the CLOCK pin of the ISP1505 using an oscilloscope. A 60 MHz clock must be observed.
8. If the link cannot perform any TXCMD, check whether the RESET_N pin is LOW during operation.
9. If the high-speed eye pattern fails, try a few samples to confirm that it is not a soldering issue.
10. If the preceding steps do not help resolve the problem, send e-mail to customer support at wired.support@philips.com, quoting the chip version, chip revision and board information.

5. PCB guideline

The ISP1505 eval board has four layers. The top and bottom layers consist of signal, power tracks and ground fill, while the second and third layers are power and ground planes.

It is recommended that you follow these guidelines when designing a transceiver PCB board:

- To get stable band gap reference V_{REF}, place the R_{RREF} resistor close to pin 4 of the ISP1505. The 12 kΩ resistor connected to RRREF must have a tight tolerance 1 % or better.
- Place decoupling capacitors close to supply pins of the ISP1505. Each $V_{CC(I/O)}$ pin must be decoupled using one decoupling capacitor. If there is a high-radiated emission, ferrite beads can be used, and must be placed close to supply pins $V_{CC(I/O)}$ and V_{CC}. Ferrite beads used in the application can be between 50 Ω and 120 Ω at 100 MHz, with a current rating of approximately 200 mA.
- Place decoupling and filtering capacitors close to the output pins of the 1.8 V and 3.3 V internal regulators.
- Place crystal and load capacitors close to XTAL1 and XTAL2 of the IC to avoid unstable oscillation because of resonance from parasitic inductance and capacitance.
- To achieve differential impedance of 90 Ω on the DP and DM lines, the trace width and spacing of DP and DM must comply with *Universal Serial Bus Specification Rev. 2.0* requirement of 7.5 mils width and 7.5 mils spacing. Also, the parallelism of the DP and DM lines should be maintained. Avoid stubs on lines.
- Ground vias are recommended for ground plane interconnect and must be kept apart by a maximum distance of 10 mm x 10 mm.
- The exposed die pad at the bottom of the ISP1505 is a ground and therefore, must be grounded on the PCB board for the transceiver to function properly.
- Route the clock out away from the data line to avoid crosstalk. If the clock signal is extremely distorted by reflection, series termination resistor can be considered. The termination resistor must be placed closed to the clock source.

6. Components required when integrating

Table 2: provides components that are required when integrating the ISP1505 into the system. For more information, refer to the ISP1505 data sheet.

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Table 2: Components required when integrating the ISP1505

Designator	Component description	Location	Value	Remark
R500	Resistor for band gap reference	On RREF (pin 4)	12 kΩ ± 1 %	-
C500	Filtering capacitor	On V_{BUS}/FAULT (pin 8)	See Table 3:	-
C503	Decoupling capacitor	On REG3V3 (pin 9)	100 nF	-
C504	Filtering capacitor	On REG3V3 (pin 9)	4.7 µF	-
Q500	Crystal oscillator	Between XTAL1 and XTAL2 (pins 10 and 11)	ISP1505/A: 19.2 MHz ± 50 ppm ISP1505/C: 26 MHz ± 50 ppm	Not required if using the clock from another source
C501, C502	Load capacitor	Between XTAL1 and XTAL2 (pins 10 and 11)	18 pF	Not required if using clock from another source
C505	Decoupling capacitor	On REG1V8 (pin 13)	100 nF	-
C506	Filter capacitor	On REG1V8 (pin 13)	4.7 µF	-
C518	Decoupling capacitor for $V_{CC(I/O)}$	On $V_{CC(I/O)}$ (pins 3 and 23)	100 nF	-
C511	Decoupling capacitor for V_{CC}	On V_{CC} (pin 7)	100 nF	-
IC504	V_{BUS} power switch	Between PSW_N/RESET_N and V_{BUS}/FAULT	Any type of the V_{BUS} power switch designed for USB applications	Required only if the transceiver is designed as a host
R511	Pull-up resistor	On PSW_N/RESET_N (pin 12)	10 kΩ	Required if the V_{BUS} power switch is needed in the design

Table 3: Recommended V_{BUS} capacitor

These values are according to the Universal Serial Bus Specification Rev. 2.0 and On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a requirements.

CV_{BUS}	Min	Max	Unit
Host	120	-	µF
Peripheral	1	10	µF

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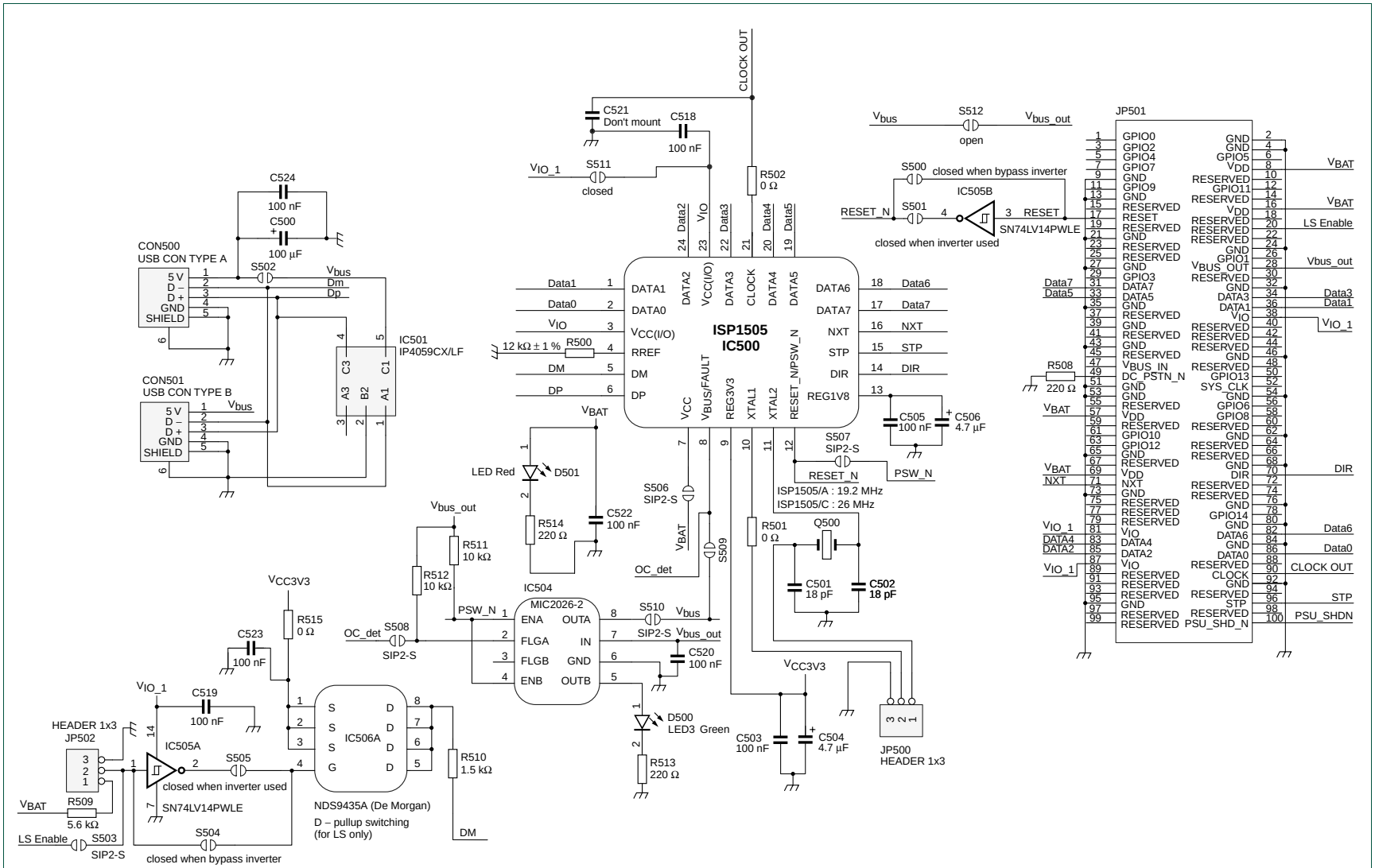

Fig 4. Schematics – part 1

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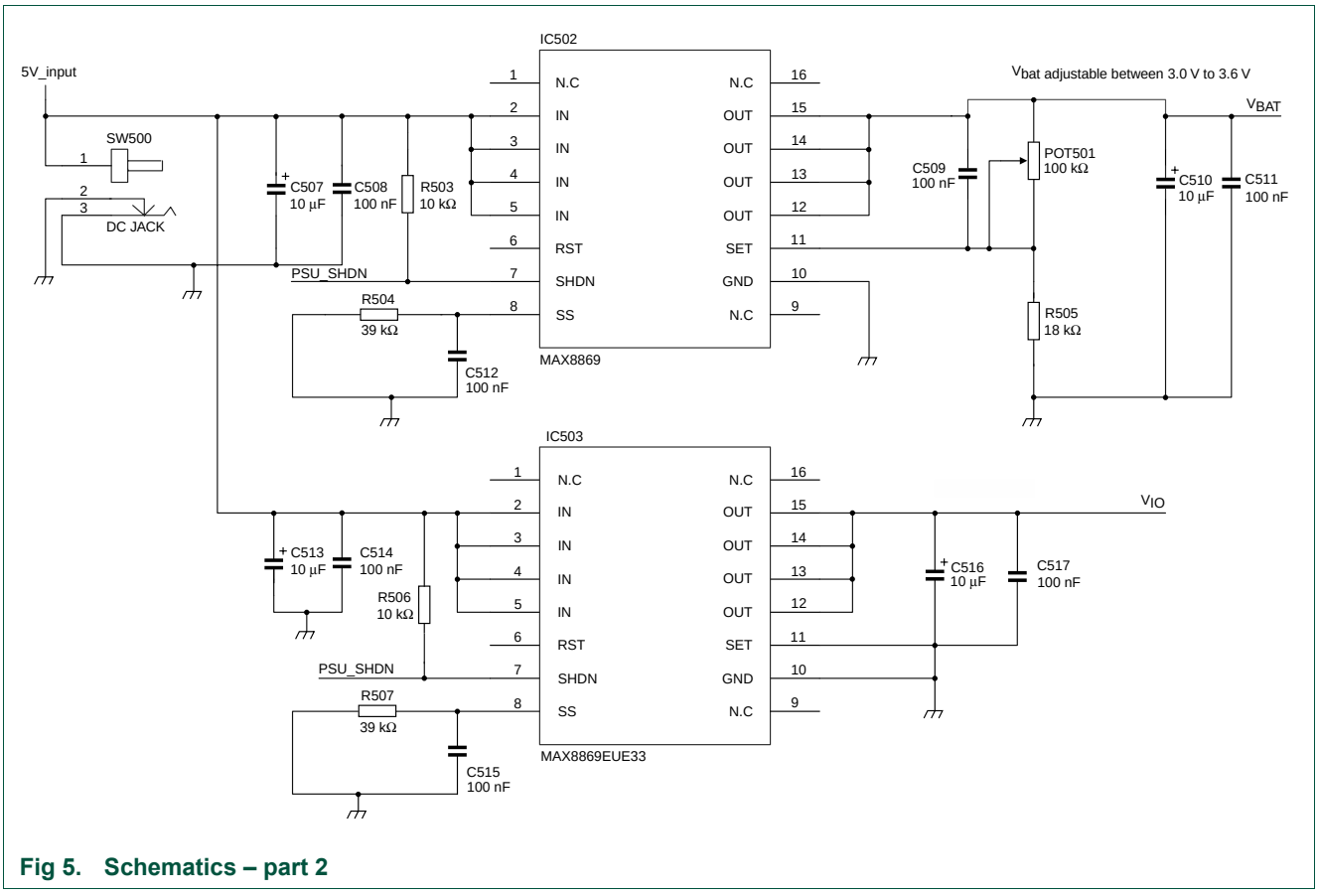

Fig 5. Schematics – part 2

7. Bill of materials

Table 4: Bill of materials

Designator	Footprint	Comment
R501 R502 R515	0603	0 Ω
C504 C506	CASE-B	4.7 µF
R503 R506 R511 R512	0603	10 kΩ
C508 C509 C511 C512 C514 C515 C517 C518 C519 C520 C522 C523 C524 C503 C505	0603	100 nF
R500	0603	12 kΩ ± 1 %
R505	0603	18 kΩ
R510	0603	1K5
C501 C502	0603	18 pF
R508 R513 R514	0603	220 Ω
R504 R507	0603	39 kΩ
JP501	2-557101-5	100PIN_T&MT
C507 C510 C513 C516	CASE B	10 µF

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Designator	Footprint	Comment
C500	CASE D	100 µF
C521	0603	Not mounted
R509	0603	5K6
Q500	Crystal	19.2 MHz
SW500	DC JACK	DC JACK
IC500	HVQFN24-SMT	ISP1505
IC501	IP4059CX5	IP4059CX/LF (optional)
S500 S501 S502 S503 S504 S505 S506 S507 S508 S509 S510 S511 S512	SIP2-S	Solder bridge
JP500 JP502	SIP3	Header 1x3
IC506	SO-8	NDS9435A
IC502	TSSO5X6-G16	MAX8869
IC503	TSSO5X6-G16	MAX8869EUE33
IC505	TSS05x6-G14/X.3	SN74LV14PWLE
IC504	SOP_8	MIC2026
CON500	USB_A	USB CON TYPE A
CON501	USB_B	USB CON TYPE B
POT501	VARR	100 kΩ
D500 D501	3MM_LED	LED3

8. Abbreviations

Table 5: Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate-Array
OTG	On-The-Go
PCB	Printed-Circuit Board
T&MT	Transceiver and Macrocell Tester
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
USB	Universal Serial Bus

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9. References

- Universal Serial Bus Specification Rev. 2.0
- ISP1505 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet
- On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a
- UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1
- USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2

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Date of release:2 May 2006

Published in The Netherlands